

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-20 (Canceled):

Claim 21 (Currently Amended): A semiconductor device having an access time measuring test mode, comprising:

- a circuit block to which an input signal is input at a timing in accordance with an input clock, and which outputs an output signal having a value corresponding to said input signal;

- a first signal path for guiding a test input signal, which has been supplied to a first pad, from said first pad to a signal input terminal of said circuit block;

- a second signal path for guiding a test clock, which has been supplied to a second pad, from said second pad to a clock input terminal of said circuit block;

- a third signal path for guiding a test output signal, which has been output from a signal output terminal of said circuit block, from said signal output terminal to a third pad; and

- a fourth signal path for guiding said test clock, which is input to said clock input terminal, from said clock input terminal to a fourth pad,

wherein said third and fourth signal paths are formed so that wiring delay time of said third and fourth signal paths are substantially equal,

wherein said fourth signal path has provided therein a first selector, responsive to a mode of a selection signal, that selectively supplies a prescribed signal or said test clock directly to said fourth pad, a first wiring that directly connects said clock input terminal of said circuit block to an input terminal of said first selector, and a second wiring that directly connects an output terminal of said first selector to said fourth pad,

~~wherein an output terminal of said first selector and said fourth pad are directly connected by a first wiring[[,]]~~

wherein said third signal path has provided therein a second selector which during a normal operation supplies a second prescribed signal other than said test output signal to said third pad and which during a test operation supplies said test output signal to said third pad, a third wiring that directly connects said signal output terminal of said circuit block to an input terminal of said second selector, and a fourth wiring that directly connects an output terminal of said second selector to said third pad, and

~~wherein an output terminal of said second selector and said third pad are directly connected by a second wiring~~

wherein said third and fourth signal paths are provided so that a difference of timings from when said test clock is output at said fourth pad to when said test output signal is output at said third pad is indicative of an access time of said circuit block.

Claim 22 (Previously Presented): The semiconductor device according to claim 21, wherein said first signal path has provided therein a third selector which during the normal operation supplies an output signal from a preceding circuit block to said signal input terminal of said circuit block, and which during the test operation supplies said test input signal to said signal input terminal of said circuit block.

Claim 23 (Previously Presented): The semiconductor device according to claim 21, wherein said second signal path has provided therein a third selector which during the normal operation supplies a normal clock to said clock input terminal of said circuit block, and which during the test operation supplies said test clock to said clock input terminal of said circuit block.

Claims 24-43 (Canceled)

Claim 44 (New): The semiconductor device according to claim 21, wherein the wiring delay time of said third and fourth signal paths are set to be substantially equal whereby a sum of lengths of said first and second wirings is set to be substantially the same as a sum of lengths of said third and fourth wirings.